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Ali Jahanian

Computer Science and Engineering / Computer and Network Architecture

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Education

■ Ph.D: Amirkabir University of Technology, Computer Engineering

Research Interests

■

■

Professional Experiences

■ , 1397→1400

■ , 1394→1395

■ , 1393→1394

■ , 1391→1394

■ , 1388→Now

Books

■ الکترونیک دیجیتال
علی جهانیان
دانشگاه شهیدبهشتی – تهران، ایران، ۱۳۹۱، شابک: ۹۷۸۹۶۴۴۵۷۲۴۳۲

Industry Collaborations

■ ابزار پایش و ارتقاء امنیت چینش تراشه
1394

■ موازی سازی الگوریتم های تولیدچینش مدارهای مجتمع روی سیستم های چند هسته ای
1389

Journal Papers

■ Systematic Trojan Detection in Crypto-Systems using the Model Checker
Hamed Hossein talaee, Ali Jahanian
JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS, Vol.3, pp. 1-20, 2024

■ Cross-Device Deep Learning Side-Channel Attacks using Filter and Autoencoder
Maryam Sadat Tabaeifard, Ali Jahanian
ISeCure-ISC International Journal of Information Security, Vol.23, pp. 149-158, 2023

■ RTL2DNA: an Automatic Flow of Large-Scale DNA-based Logic Circuit Design
Zohreh Beiki, Ali Jahanian
Scientia Iranica, pp. 1-25, 2022

■ Generic and Scalable DNA-based Logic Design Methodology for Massive Parallel Computation
Zohreh Beiki, Ali Jahanian
JOURNAL OF SUPERCOMPUTING, Vol.79, pp. 1426-1450, 2022

■ A Time Randomization based Countermeasure against the Template Side Channel Attack
Farshideh Kordi, Hamed Hossein talaee, Ali Jahanian
ISeCure-ISC International Journal of Information Security, Vol.14, pp. 47-55, 2022

■ Intensive Analysis of Physical Parameters of Power Sensors for Remote Side-Channel Attacks
Milad Salimian, Ali Jahanian
ISeCure-ISC International Journal of Information Security, Vol.13, pp. 163-176, 2021

■ Analytical design of multi-threshold and high fan-in DNA-based logical sensors to profile the pattern of MS microRNAs
Mercedeh Sanjabi, Ali Jahanian
Biomedical Engineering Letters, Vol.11, pp. 131-145, 2021

■ Power side-channel leakage assessment and locating the exact sources of leakage at the early stages of ASIC design process
Vahhab Samadi Bokharaie, Ali Jahanian
JOURNAL OF SUPERCOMPUTING, Vol.113, pp. 2219-2244, 2021

■ Multi-input DNA-based Logic Gates for Profiling the microRNA Biomarkers of Hepatitis-C Viral Infection
Melika sadat Masoud, Mercedeh Sanjabi, Ali Jahanian
Journal on Computer Science and Engineering, Vol.18, pp. 16-23, 2021

■ Side-channel leakage assessment metrics and methodologies at design cycle: A case study for a cryptosystem
Vahhab Samadi Bokharaie, Ali Jahanian
Journal of Information Security and Applications, Vol.54, 2020

■ A Customized Digital Microfluidic Biochip Architecture/CAD flow for Drug Discovery Applications
Shadi Momtahen, Taajobian Maryam, Ali Jahanian
IEEE Nanotechnology Magazine, Vol.13, pp. 25-34, 2019

■ RNA Secondary Structured Logic Gates for Profiling the microRNA Cancer Biomarkers
Mahsa Yazdani, Zohreh Beiki, Ali Jahanian
IET Nanobiotechnology, Vol.14, pp. 181-190, 2019

■ Multi-threshold and Multi-input DNA Logic Design Style for Profiling the MicroRNA Biomarkers of Real Cancers
Mercedeh Sanjabi, Ali Jahanian
IET Nanobiotechnology, Vol.13, pp. 665-673, 2019

■ Drug Discovery Acceleration using Digital Microfluidic Biochip Architecture and computer-aided-design flow
Shadi Momtahen, Taajobian Maryam, Ali Jahanian
International Journal of Engineering, Vol.32, pp. 1169-1176, 2019

■ Massive Parallel Digital Micrflouidic Biochip Architecture for Automating Large-Scale Biochemistry Assays
Abbas Haddad, Maryam Taajobian, Ali Jahanian
Scientia Iranica, Vol.25, pp. 3461-3474, 2018

■ Real Parallel and Constant Delay Logic Circuit Design Methodology based on the DNA Model-of-Computation
Zohreh Beiki, Zahra Zare Dorabi, Ali Jahanian
MICROPROCESSORS AND MICROSYSTEMS, Vol.61, pp. 217-226, 2018

■ Improved Experimental Time of Ultra large Bioassays using a Parallelized Microfluidic Biochip Architecture/Scheduling
Maryam Taajoban, Ali Jahanian
IET Nanobiotechnology, Vol.4, pp. 484-490, 2017

■ Three-dimensional Physical Design Flow for Monolithic 3D-FPGAs to Improve Timing Closure and Chip Area Systems
Armin Belghadr, Ali Jahanian
JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS, Vol.26, 2017

■ DENA A Configurable Micro-architecture and Design Flow for Bio-medical DNA-based Logic Design
Zohreh Beiki, Ali Jahanian
IEEE Transactions on Biomedical Circuits and Systems, Vol.11, pp. 1077-1086, 2017

■ Customized Placement Algorithm of Nanoscale DNA Logic Circuits
Sedighe Farhadtoosky, Ali Jahanian
JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS, Vol.26, 2017

■ Self Authentication Path Insertion in FPGA-based Design Flow for Tamper-resistant Purpose
SHARAREH ZAMANZADEH, Ali Jahanian
ISeCure-ISC International Journal of Information Security, Vol.8, pp. 53-60, 2016

■ ASIC Design Protection against Reverse Engineering during the Fabrication Process using Automatic Netlist Obfuscation Design Flow
SHARAREH ZAMANZADEH, Ali Jahanian
ISeCure-ISC International Journal of Information Security, Vol.8, pp. 87-98, 2016

■ Higher Security of ASIC Fabrication Process Against Reverse Engineering Attack using Automatic Netlist Encryption Methodology
SHARAREH ZAMANZADEH, Ali Jahanian
MICROPROCESSORS AND MICROSYSTEMS, Vol.42, pp. 1-9, 2016

■ Higher Flexibililty of Reconfigurable Digital Micro/Nano Fluidic Biochips using an FPGA-Inspired Architecture
, Ali Jahanian
Scientia Iranica, Vol.23, pp. 1554-1562, 2016

■ Security Path an Emerging Design Methodology to Protect the FPGA IPs against Passive/Active Design Tampering
SHARAREH ZAMANZADEH, Ali Jahanian
JOURNAL OF ELECTRONIC TESTING-THEORY AND APPLICATIONS, Vol.32, pp. 329-343, 2016

■ Security-aware Register Placement to Hinder Malicious Hardware Updating and Improve Trojan Detectability
, Ali Jahanian
isesco journal of science and technology, Vol.7, pp. 1-7, 2015

■ Three-dimensional Switchbox Multiplexing in Emerging 3D-FPGAs to Reduce Chip Footprint and Improve TSV Usage
Marzieh Morshedzadeh, Ali Jahanian, Payam Poor Ashraf
INTEGRATION-THE VLSI JOURNAL, Vol.50, pp. 81-90, 2015

■ High Performance CMOS (4 2) compressor
, Ghassem Jaberipur, Ali Jahanian
Taylor Francis, 2014

■ A Fast Placement Algorithm for Embedded Just-In-Time Reconfigurable Extensible Processing Platform
Seyedhassan Daryanavard, Mohammad Eshghi, Ali Jahanian
JOURNAL OF SUPERCOMPUTING, Vol.71, pp. 121-143, 2014

■ Improved Delay and Process Variation Tolerance of Clock Tree Network in Ultra-large Circuits using Hybrid RF/Metal Clock Routing
, Ali Jahanian
JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS, Vol.23, pp. 1-19, 2014

■ Metro-on-FPGA a feasible solution to improve the congestion and routing resource management in future FPGAs
Armin Belghadr, Ali Jahanian
INTEGRATION-THE VLSI JOURNAL, Vol.47, pp. 96-104, 2014

■ High Performance CMOS (4 2) Compressors
Abdoreza Pishvaie, Ghassem Jaberipur, Ali Jahanian
INTERNATIONAL JOURNAL OF ELECTRONICS, Vol.101, pp. 1511-1525, 2014

■ Redesigned CMOS (4 2) compressor for fast binary multipliers
, Ghassem Jaberipur, Ali Jahanian
CANADIAN JOURNAL OF ELECTRICAL AND COMPUTER ENGINEERING-REVUE CANADIENNE DE GENIE ELECTRIQUE ET INFORMATIQUE, Vol.36, pp. 111-115, 2014

■ Trojan Vulnerability Map an Efficient Metric for Modeling and Improvement of Hardware Security Level
Abdolmahmood Bakhshizadeh, Ali Jahanian
IEICE TRANSACTIONS ON FUNDAMENTALS OF ELECTRONICS COMMUNICATIONS AND COMPUTER SCIENCES, Vol.95, pp. 1-9, 2012

■ Performance Improvement and Congestion Reduction of Large FPGAs using On-chip Microwave Interconnects
Armin Belghadr, Ali Jahanian
IEICE TRANSACTIONS ON COMMUNICATIONS, Vol.95, pp. 1610-1618, 2012

■ Improved CMOS (4 2) compressor designs for parallel multipliers
, Ghassem Jaberipur, Ali Jahanian
COMPUTERS and ELECTRICAL ENGINEERING, Vol.38, pp. 1703-1716, 2012

■ Improved Line Tracking System for Autonomous Navigation of
Yahya Zare Khafri, Ali Jahanian
INTERNATIONAL JOURNAL OF ROBOTICS and AUTOMATION, Vol.30, pp. 25-30, 2012

■ Improved Timing Closure by Analytical Buffer and TSV Planning in Three-dimensional Chips
Ali Jahanian, rEZA Abdollahi
IEICE ELECTRONICS EXPRESS (MSRT BLACKLIST), Vol.9, pp. 1849-1854, 2012

■ Parallelizing the FPGA Global Routing Algorithm on Multi-core Systems without Quality Degradation
, Ali Jahanian
IEICE ELECTRONICS EXPRESS (MSRT BLACKLIST), Vol.24, pp. 2061-2067, 2011

■ Using chip master planning in automatic ASIC design flow to improve performance and buffer resource management
Ali Jahanian,
Journal of computer and robotics, pp. 125-135, 2011

■ Comparative Performance Evaluation of Large FPGAs with CNFET- and CMOS based Switches in Nanoscale
, Ali Jahanian, Keyvan Navi
JOURNAL NANO MICRO LETTERS, Vol.3, 2011

■ Comparative Performance Evaluation of Large FPGAs with CNFET- and CMOS-based Switches in Nanoscale
, Ali Jahanian, - -
JOURNAL NANO MICRO LETTERS, Vol.3, pp. 177-178, 2011

■ Comparative Performance Evaluation of Large FPGAs with CNFET and CMOS based Switches in Nanoscale
Mohammad Hossein Moaiyeri, Ali Jahanian, Keyvan Navi
Nano-Micro Letters, Vol.3, pp. 178-188, 2011

■ Improved predictability timing yield and power consumption using hierarchical highways-on-chip planning methodology
Ali Jahanian, Morteza Saheb zamani, Hamid Safizadeh
INTEGRATION-THE VLSI JOURNAL, Vol.44, pp. 123-135, 2011

■ Early buffer planning with congestion control using buffer requirement map
Ali Jahanian, Morteza Saheb zamani
JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS, Vol.5, pp. 949-973, 2010

■ A Landmark-based Navigation System for High Speed Cars in the Roads with Branches
Mercedeh Sanjabi, Somayeh Maabi, Ali Jahanian,
International Journal of Information Acquisition (IJIA), Vol.6, pp. 193-202, 2009

■ An Improved Standard Cell Placement Methodology using Hybrid Analytic and Heuristic Techniques
Ali Jahanian, ,
ADVANCES IN COMPUTER SCIENCE AND ENGINEERING, Vol.6, 2009

■ Higher routability and reduced crosstalk noise by asynchronous multiplexing of on-chip interconnects
Ali Jahanian, Morteza Saheb zamani
Scientia Iranica, Vol.17, 2009

■ Using metro-on-chip in physical design flow for congestion and routability improvement
Ali Jahanian, Morteza Saheb zamani
MICROELECTRONICS JOURNAL, Vol.39, pp. 261-274, 2008

■ Evaluating the Metro-on-Chip Methodology to Improve the Congestion and Routability
Ali Jahanian, Mostafa Rezvani, Morteza Saheb zamani, Mehrdad Najibi
Advances in Computer and Information Sciences and Engineering, pp. 689-696, 2008

■ Metro-on-Chip an efficient physical design technique for congestion reduction
Ali Jahanian, Morteza Saheb zamani
IEICE ELECTRONICS EXPRESS (MSRT BLACKLIST), Vol.4, pp. 510-516, 2007

■ Evaluation prediction and reduction of routing congestion
Mahdi Saeedi, Ali Jahanian, Morteza Saheb zamani
MICROELECTRONICS JOURNAL, Vol.38, pp. 942-958, 2007

■ قرنطینه سازی تروجانهای سخت افزاری در پردازنده های عام منظوره با روشهای نرم افزاری مبتنی بر مترجم
فرزانه قطب الدینی قاسم آباد، علی جهانیان
علوم رایانش و فناوری اطلاعات، نسخه ۱۷، صفحات: ۵۲-۶۱، ۱۳۹۸

■ DNA جهت تشخیص زودهنگام سرطان با استفاده از دروازه های منطقی miRNA بررسی میزان بیان
طاهره یحیی، شهره زارع کاریزی، علی جهانیان
دانشگاه علوم پزشکی اراک، نسخه ۹، صفحات: ۹۶-۱۰۹، ۱۳۹۵

■ طرح ریزی اتصالات امواج رادیویی روی مدارهای مجتمع خاص منظوره با هدف بهبود
زارعی علی محمد ، علی جهانیان
نسخه ۹، صفحات: ۳۴-۴۱، ۱۳۸۹، the csi journal of computer science and engineering

■ توزیع مناسب منابع بافر با طرح ریزی بافرها در سطح جاسازی با هدف کاهش تعداد بافر و مدیریت تراکم
علی جهانیان، مرتضی صاحب الزمانی
نسخه ۵، صفحات: ۱۲-۲۲، ۱۳۸۵، the csi journal of computer science and engineering

Conference Papers

■ Real Vulnerabilities in Partial Reconfigurable Design Cycles; Case Study for Implementation of Hardware Security Modules
Hanieh Jafarzadeh, Ali Jahanian
2020 20th International Symposium on Computer Architecture and Digital Systems (CADS)

■ Protecting the FPGA IPs against Higher-order Side Channel Attacks using Dynamic Partial Reconfiguration
Ario Kianazad, Hamed Hossein talaee, Ali Jahanian
2020 20th International Symposium on Computer Architecture and Digital Systems (CADS), pp.1-6

■ Vulnerability Analysis Against Fault Attack in terms of the Timing Behavior of Fault Injection
Mahbube Fakhire, Ali Jahanian
2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp.374-379

■ High Accuracy Multi-input DNA Logic Gate using the Spatially Localized DNA structures
Ehsan Jamalzadeh, Ali Jahanian
CSICC 2020

■
Farzaneh Ghobaddini ghasem abad, Ali Jahanian
CSICC 2020

■ Security Improvement of FPGA Design Against Timing Side Channel Attack Using Dynamic Delay Management
Bayat-Makou Pourya, Ali Jahanian, Reshadi Media
IEEE Canadian Conference on Electrical Computer Engineering (CCECE)

■ Efficient Mapping of DNA Logic Circuits on Parallelized Digital Microfluidic Architcture
Zohreh Beiki, Maryam Taajobian, Ali Jahanian
19th International Symposium on Computer Architecture and Digital Systems (CADS), pp.93-98

■ Scalable Security Path Methodology A Cost-security Trade-off to Protect FPGA IPs against Active and Passive Tampers
SHARAREH ZAMANZADEH, Ali Jahanian
Asian Hardware Oriented Security and Trust Symposium (AsianHOST), pp.85-90

■ High-Performance General-Purpose Arithmetic Operations using the Massive Parallel DNA-based Computation
Mercedeh Sanjabi, Ali Jahanian, Maryam Tahmasbi
EuroMicro Digital System Design (DSD2017), pp.543-546

■ Layout Vulnerability Reduction against Trojan Insertion using Security-aware White Space Distribution
Hamed Hossein Talaee, Ali Jahanian
International Symposium on VLSI (ISVLSI), pp.551-555

■ A new Cell Placement Algorithm for Localized DNA Logic Circuits Mounted on Origami Surface
Sedighe Farhadtoosky, Ali Jahanian
International Conference on DNA Computing and Molecular Programming (DNA22), pp.102-104

■
, Ali Jahanian
1st International Conference on New Research Achievements in Electrical and Computer Engineering, pp.436-443

■ Isolating the Register-bank Trojans in General-purpose Microprocessors using Secure Programming
Peyman Talebian, Ali Jahanian
1st International Conference on New Research Achievements in Electrical and Computer Engineering

■ Fault-tolerant architecture and CAD algorithm for field-programmable pin-constrained digital microfluidic biochips
Alireza Abdoli, Ali Jahanian
CSI Symposium on Real-Time and Embedded Systems and Technologies (RTEST)

■
Bahareh Ahmadi Haji, Mehrshad Vosoughi, Ali Jahanian

12th International ISC conference on Information security and cryptology

■
SHARAREH ZAMANZADEH, Ali Jahanian
12th International ISC conference on Information security and cryptology

■ DENA a Configurable Architecture for Multi-stage DNA Logic Circuit Design
Zohreh Beiki, Ali Jahanian
International Conference on DNA Computing and Molecular Programming (DNA21), pp.17-18

■ Improved performance and resource usage of FPGA using resource-aware design the case of decimal array multiplier
Adel Hosseiny, Saba Amanollahi Baharvand, Ali Jahanian
International Symposium on Computer Architecture and digital systems (CADS), pp.121-122

■ A General-Purpose Field-Programmable Pin-Constrained Digital Microfluidic Biochip
Ali Jahanian
International Symposium on Computer Architecture and digital systems (CADS)

■ RF resource planning in application specific integrated circuits to improve timing closure
, Ali Jahanian
International Symposium on Computer Architecture and digital systems (CADS), pp.131-132

■
SHARAREH ZAMANZADEH, Ali Jahanian
21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), pp.52-53

■ EJOP an extensible Java processor with reasonable performance/flexibility trade-off
, , Ali Jahanian
EuroMicro Digital System Design(DSD), pp.415-418

■ RF-Interconnect resource assignment and placement algorithms in application specific ICs to improve performance and reduce routing congestion
Ali Jahanian, Bahareh Poorshirazi
Euromicro conference on digital system design

■ Multiplexed switch box architecture in three-dimensional FPGAs to reduce silicon area and improve TSV usage
Marzieh Morshedzadeh, Ali Jahanian
Great Lakes Symposium on VLSI (GLSVLSI)(2012), pp.303-306

■ ParSA parallel simulated annealing placement algorithm for multi-core systems
, Ali Jahanian, Saba Amanollahi Baharvand, Negar Niralaee
International Symposium on Computer Architecture and Digital Systems (CADS)

■ Modeling evaluation and mitigation of SEU error in three-dimensional FPGAs
, Ali Jahanian,
International Symposium on Computer Architecture and Digital Systems (CADS)

■ Improved performance and power consumption of three-dimensional FPGAs using Carbon Nanotube interconnects
, Ali Jahanian
International Symposium on Computer Architecture and Digital Systems (CADS)

■ Edu3 a simple and efficient platform for education of three-dimensional physical design automation algorithms
Ali Jahanian, Saba Amanollahi Baharvand
Design Automation and test(Date)

■ EduCAD an Efficient Flexible and Easily Revisable Physical Design Tool for Educational Purposes
Ali Jahanian, Saba Amanollahi Baharvand
Design Automation and test(Date)

■ Landmark-based car navigation with overtake capability in multi-agent environments
, , Ali Jahanian,

■ VMAP a variation map-aware placement algorithm for leakage power reduction in FPGAs
, , Ali Jahanian
14th euromicro conference on Digital System Design(DSD)

■ A CNT/Metal Hybrid Routing Architecture to Improve Performance of Ultra-Large FPGAs
, Ali Jahanian
International Conference on Computer Design and Engineering (ICCDE) (2011)

■ feasibility study of using the rf interconects in large fpgas to improve routing tracks usage
, Ali Jahanian, Esfandiar Mehrshahi, Mohammad Taghi Teimoori
2011IEEE COMPUTER SOCIETY ANNUAL SYMPOSIUM ON VLSI

■ Congestion and Track Usage Improvement of Large FPGAs Using Metro-on-FPGA Methodology
, , Ali Jahanian
Great Lakes Symposium on VLSI (GLSVLSI) (2011), pp.49-54

■ Chip master planning an efficient methodology to improve design closure and complexity management of ultra large chips
Ali Jahanian
CSI Internationa Symposium on Computer Architecture and Digital Systems(CADS)

■ A thermal-aware delay model for pass transistor in FPGA switch boxes
, Ali Jahanian, , Morteza Saheb zamani

■ A light - weght car navigation algorithm for high speed agents using wireless landmarks
, Ali Jahanian,
ICIA 2009 IEEE International Conference on Information and Automation

■ multi -domain clock skew scheduling - Aware register placementto optimize clock distribution network
, , Ali Jahanian,
date (design automation test in europe

■ improved performance and yield whih chip master planingdesign methodology
Ali Jahanian,
GLSVLSI

■ Improved timing closure by early buffer planning in floor-placement design flow
Ali Jahanian, Morteza Saheb zamani
GLSVLSI, pp.558-563

■ Improved performance and yield with Chip Master planning design methodology
Ali Jahanian,
Great Lakes Symposium on VLSI (GLSVLSI) (2009)

■ Performance and timing yield enhancement using Highway-on-Chip Planning
Ali Jahanian
EuroMicro Digital System Design(DSD)

■ Performance improvement of physical retiming with shortcut insertion
Adel Dokhanchi, Mostafa Rezvani, Ali Jahanian, Morteza Saheb zamani
IEEE computer society annual symposium on VLSI, pp.215-220

■ Multi-level buffer block planning and buffer insertion for large design circuits
Ali Jahanian, Morteza Saheb zamani
IEEE computer society annual symposium on VLSI, pp.411-415

■ Using asynchronous serial transmission in physical design for congestion reduction
Ali Jahanian
IEEE East-West Design and Test Conference

■ Prediction and reduction of routing congestion
Ali Jahanian
International Symposium on Physical Design(ISPD)

■ Efficient host-independent coprocessor architecture for speech coding algorithms
Ali Jahanian
EuroMicro Digital System Design(DSD)

■ An efficient congestion reduction algorithm based on contour plotting
Ali Jahanian
International Conference on Microelectronics

■ Congestion prediction from metric definition to routing estimation
Ali Jahanian
International Conference on Microelectronics

■ Area efficient low power and robust design for add-compare-select units
Ali Jahanian
EuroMicro Digital System Design(DSD)

■ Ant colony solution dynamic Steiner tree problem
علی نور اللّه، علی جهانیان، ادیبی پیمان ، هاشمی تشکری سید مهدی
هفتمین کنفرانس انجمن کامپیوتر ایران

■ ارائه یک روش نقاب گذاری ریزدانه جهت مقاوم سازی تراشه های خاص منظوره در برابر حملات کانال جانبی
وهاب صمدی بخارائی، علی جهانیان
بیست و هفتمین کنفرانس بین المللی کامپیوتر، انجمن کامپیوتر ایران

■ Flexible and Automatable Microfluidic-based Architecture and CAD Algorithm for Implementation of Large DNA Digital Storage
مصطفی پوراسداله، مریم تعجبیان، علی جهانیان
بیست و هفتمین کنفرانس بین المللی کامپیوتر، انجمن کامپیوتر ایران

■ OVR: a Practical Metric for Vulnerability Assessment of Digital Circuits against Side-channel Attacks
وهاب صمدی بخارائی، علی جهانیان
سیزدهمین کنفرانس ملی فرماندهی و کنترل

■ Cost-Effective and Practical Countermeasure against the Template Side Channel Attack
فرشیده کردی، حامد حسین طلائی، علی جهانیان
هفدهمین کنفرانس بین المللی انجمن رمز ایران، صفحات:۵۴-۶۰

■ Analysis of Geometrical Parameters for Remote Side-Channel Attacks on Multi-Tenant FPGAs
میلاد سلیمیان، علی جهانیان
هفدهمین کنفرانس بین المللی انجمن رمز ایران، صفحات:۲۱-۲۹

■ A New Nano-scale Differential Logic Style for Power Analysis Attack
عبدی امید، علی جهانیان
بیست و ششمین کنفرانس ملی مهندسی برق

■ DNA با استفاده از دروازه منطقی C تشخیص الگوی زیست نشانگرهای گسترش عفونت ویروسی هپاتیت

ملیکاسادات مسعود، علی جهانیان
بیست و سومین کنفرانس ملی سالانه انجمن کامپیوتر ایران

■ Security Improvement of FPGA Configuration File Against the Reverse Engineering Attack
شهرام شهابی آهنگر کلایی، شراره زمان زاده، علی جهانیان
سیزدهمین کنفرانس بین المللی انجمن رمز ایران، صفحات: ۱۰۱-۱۰۵

■ Drug Discovery Evolution Using the Customized Digital Microfluidic Biochips
شادی ممتحن، مریم تعجبیان، علی جهانیان
بیست و چهارمین کنفرانس مهندسی برق ایران

■ Design of CAD ASIP for JIT extensible processor Case study on PathFinder routing algorithm
سیدحسن دریانورد، محمد عشقی، علی جهانیان
بیست و سومین کنفرانس مهندسی برق ایران

■ ارائه یک معماری برنامه پذیر جدید برای تراشه های زیستی ریز سیال دیجیتال
عباس حداد، تعجبیان مریم، علی جهانیان
بیست و دومین کنفرانس مهندسی برق ایران ICEE۲۰۱۴

■ ارائه الگوریتم افراز موازی و پیاده سازی آن روی واحد پردازش گرافیکی
سیده عاطفه طاهری تاری، علی جهانیان
بیست و دومین کنفرانس مهندسی برق ایران ICEE۲۰۱۴

■ Design of CAD ASIP for JIT extensible processor case study on Simulated Annealing placer
علی جهانیان
بیست و دومین کنفرانس مهندسی برق ایران ICEE۲۰۱۴

■ ارائه یک کتابخانه صنعتی سلول های استاندارد براساس فناوری نانولوله های کربنی
محمد جرنگی، علی جهانیان، مهیا سام دلیری، محمدحسین معیری
نوزدهمین کنفرانس ملی سالانه انجمن کامپیوتر ایران، صفحات: ۹۵۰-۹۵۵

■ جلوگیری از درج ویروس های سخت افزاری با ارائه یک معماری جدید برای درخت سیگنال ساعت
مهرشاد وثوقی، علی جهانیان
هجدهمین کنفرانس ملی سالانه انجمن کامپیوتر ایران

■ طرح ریزی اتصالات امواج رادیویی روی مدارهای مجتمع خاص منظوره با هدف بهبود کارایی
علی محمد زارعی، علی جهانیان
هجدهمین کنفرانس ملی سالانه انجمن کامپیوتر ایران

■ Clock tree network using hybrid RF/metal clock routing
زهره محمدی ارفع، علی جهانیان
(سمینار الکترونیک و فرصت های فرارو (دانشگاه صنعتی شریف

■ A new nanowire-based FPGA to improve routing congestion and routability

آرش فرکیش، علی جهانیان
(سمینار الکترونیک و فرصت های فرارو (دانشگاه صنعتی شریف

■ TrueFlex A Flexible and Efficient Evaluation Platform for Networked Automotive Systems
سیدعلی مرعشی، علی جهانیان
ICEE۲۰۱۲بیستمین کنفرانس مهندسی برق ایران

■ Design implementation and improvement of decimal parallel multiplier on ASIC and FPGA
امین ملک پور، ملک پور سعید، علی جهانیان
ICEE۲۰۱۲بیستمین کنفرانس مهندسی برق ایران

■ ارائه ی معماری و دستورات سفارشی جدید برای سفارشی سازی معماری پردازنده ی جاوا با هدف بهبود کارایی این نوع پردازنده
ابوالقاسمی نیلوفر، طالبی سمانه، علی جهانیان، نوری حمید
ICEE۲۰۱۲بیستمین کنفرانس مهندسی برق ایران

■ Redesigned CMOS (۴ ۲) compressor for fast binary multipliers
پیشوایی عبدالرضا ، قاسم جابری پور، علی جهانیان
ICEE۲۰۱۲بیستمین کنفرانس مهندسی برق ایران

■ سه ورودی XOR سریع بر پایه دروازه CMOS طراحی کمپرسور (۴ ۲
عبدالرضا پیشوایی، قاسم جابری پور، علی جهانیان
هفدهمین کنفرانس ملی سالانه انجمن کامپیوتر ایران، صفحات: ۳۰۰-۳۰۵

■ Buffer planning using the buffer requirement map with congestion control
علی جهانیان
سیزدهمین کنفرانس بین المللی انجمن کامپیوتر ایران

■ Buffer insertion during placement with floorplanning information
علی جهانیان
دوازدهمین کنفرانس بین المللی انجمن کامپیوتر ایران

■ Feasibility of using component based software formal verification by hardware formal verification tools
علی جهانیان
یازدهمین کنفرانس انجمن کامپیوتر ایران

■ A hybrid heuristically and mathematically approach for VLSI standard cell placement
علی جهانیان
یازدهمین کنفرانس انجمن کامپیوتر ایران

■ Using On-chip RF-Interconnects to Optimize Clock Distribution Network In ۱۹th Iranian Conference on Electrical Engineering (ICEE)
علی جهانیان

نوزدهمین کنفرانس بین المللی برق ایران

■ Parallelizing the PathFinder Global Routing Algorithm using Multi-core Systems
علی جهانیان
نوزدهمین کنفرانس بین المللی برق ایران

■ Hardware-Software Co-Simulation
علی جهانیان
چهارمین کنفرانس بین المللی سالانه انجمن کامپیوتر ایران

■ بهبود ساختار جعبه سوئیچ به منظور مقاوم سازی آرایه های دروازه ای برنامه پذیر در برابر مهندسی معکوس رشته بیتی
شهرام شهابی آهنگر کلایی، علی جهانیان
کنفرانس مهندسی برق ایران

thesis and doctoral thesis

■
Fatemeh Zahra Zahedi
2022

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Mercedeh Sanjabi
2022

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Vahhab Samadi Bokharaie
2022

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Zohreh Beiki
2018

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SHARAREH ZAMANZADEH
2017

M.Sc. Theses

■ A Hardened Architecture Against the Spectre Architecture-based Attack
Zahra Athari Nikooravan
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Amin Foshati
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Milad Salimian
2020

■ Vulnerability Analysis of Design against side channel Fault Injection Attack
Mahbube Fakhire
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■ Hardware Protection against Template Attack by Managing the Information Leakage of side channel features
Farshideh Kordi
2020

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Mahsa Yazdani
2019

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Ario Kianazad
2019

■
Farzaneh Ghobaddini ghasem abad
2019

■
Hanieh Jafarzadeh
2019

■
Mahboobeh Masoudi
2019

■ Logic biosensor design based on DNA for Hepatitis diagnosis
Melika sadat Masoud

2019

■ Proposing a customized architecture and design flow for digital microfluidic biochips in drug discovery applications
Shadi Momtahen
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Pooria Sadeghi
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Mahya Morid Ahmadi
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Alireza Mashayekh
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Yahya Zare Khafri
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Awards & Honors

■ پژوهشگر نمونه سال ۱۳۹۱